Please add new claims 16 and 17 as follows:

A3 B1

--16. A semiconductor memory device according to claim 3, wherein said read data is different in bit width from said write data.

17. A semiconductor memory device according to claim 4, wherein said read data is different in bit width from said write data.--

REMARKS

Claims 2-17 are pending in this application, of which claims 3, 4, and 9 are independent. For the following reasons, this application should be considered in condition for allowance and passed to issue.

Submission of IDS

Applicant files concurrently with this amendment an IDS with the appropriate fee. Consideration of the cited reference is respectfully solicited.

Claim Amendments

Claims 3 and 4 have been amended to independent form by incorporating the subject matter claim 1. Claims 1 and 2 have been cancelled without prejudice or disclaimer of the subject matter thereof. Claim 15 has also been amended to depend from claim 3. New claims 16 and 17 have been added. Care has been taken to avoid the introduction of new matter.

Office Action Summary

The Office Action rejects claims 1-3, 9, and 11-15 under 35 U.S.C. §102(b) as being anticipated by Chappell [et al.] (U.S. Patent No. 5,204,841). The Examiner also

objects to claims 4-8 and 10 as being dependent upon a rejected base claim, but indicates that they would be allowable if rewritten in independent form.

Allowable Claims

To place claims 4-8 in an allowable condition as suggested by the Examiner, claim 4 has been rewritten in independent form by incorporating the subject matter of claim 1. Hence, claim 4 and claims dependent therefrom are now allowable. Moreover, new claim 17 has been added to depend from claim 4, and explicitly recites that bit width of the read and write data are different. Claim 17 is allowable as it depends from allowable claim 4.

Rejection of Claims 1-3, 9, and 11-15

As the claims have been amended, Applicant addresses independent claims 3 and 9 and claims 11-15 cited under the rejection.

The Examiner correlates Fig. 1 of Chappell with the claimed plurality of input terminals and alleges that the text at col. 9, lines 27-34 (which correspond to Fig. 5), discloses the claimed "at least one output terminal for outputting read data."

Fig. 1 of Chappell illustrates a high level block diagram of a multi-port RAM, in which a memory array is divided into a plurality of blocks, which are sequentially accessed in a pipelined manner. Chappell intends to implement a fast accessible multi-port memory. To accomplish this, the timings of the control signals are generated on a block by block basis, and when accessing one block is completed, then another block is accessed. Due to the generation of the timing generation in units of blocks, the access cycle within the chip is made shorter than the machine cycle.

In Chappell, each port is provided with a separate address input port, control signal input port, data input port, and data output port. The Examiner states that Chappell discloses on col. 9, lines 27-34, that write data and read data are made different in bit width from each other. We respectfully disagree.

Contrary to the claims, Chappell describes that the sub-array address bus, the word line address bus, and the bit line address bus are different in bit width. Chappell taps out the signal on the word line address bus that is the slowest among the address buses, to generate a control signal for starting the access cycle in the next block. Accordingly, the bit width and delay are different for each "address bus" that selects the sub-array, the word line, and the bit lines.

The Examiner seems to correlate the bit-width of the multiple address buses with the claimed bit-width relationship between the read and write data. While the bit-width of the respective address buses of Chappell may be different, this arrangement does not affect the bit-width of the read and write data or the number of input and output data ports. Chappell fails to disclose or suggest a relationship between the read data and the write data, a relationship between the respective bit-width of the read and write data, or a relationship between the number of input and output ports, as claimed. For instance, in Fig. 1 of Chappell, the data input terminal DI1-DIN and data output terminals DO1-DON are illustrated, however, Chappell does not specifically refer to the data bit width of the port nor the number of input ports as compared to the number of output ports. In fact, Chappell provides for the same number of input ports and output ports.

Claim 3 and Dependent Claims

Claim 3 recites, *inter alia,*

> at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data, wherein the input terminals are coupled to a first bus, and said at least one output terminal is coupled to a second bus, and each of the first and second buses is a unidirectional bus for transferring a signal or data in one direction.

Contrary to claim 3, the input and output terminals of Chappell are the same in number. There is no disclosure or suggestion of the output and input terminals being different in number, as claim 3 recites. For at least this reason, claim 3 is patentable over the Chappell reference.

New claim 16, dependent from claim 3, recites further that the read data is different in bit width from the write data. As discussed above, this feature is neither disclosed nor suggested by Chappel.

Claim 15, amended to depend from claim 3, recites further that the input terminals receive write data, the control signal, and the address signal at common terminals. Contrary to claim 15, Chappell explains that write data, the control signal, and the address signal are received from different terminals instead from a common terminal, as claim 15 recites.

For the above reasons, Applicant submits that Chappell fails to disclose or suggest each and every element of any one of claims 3, 15, and 16.

Claim 9 and Dependent Claims

Claim 9 recites:

A memory system, comprising:
a memory for storing information;
a memory controller for controlling access to said memory;
a first unidirectional bus for transferring write data, a control signal and an address signal from said memory controller to said memory; and
a second unidirectional bus for transferring read data from said memory to said memory controller, said read data being allowed to be different in bit width from said write data.

As claim 9 recites, read data is different in bit width from the bit width of write data. As discussed above, there is no disclosure or suggestion of the bit width relationship between read and write data input to respective terminals of Chappell.

Claim 9 recites further that the first unidirectional bus transfers write data, a control signal, and an address signal. Again, Chappell fails to disclose or suggest a first unidirectional bus configured in this manner. Chappell explicitly discloses separate buses of different widths for transferring the noted data and signals, but does not disclose or suggest a unidirectional bus transferring the same.

Claims 10-14 recite novel circuitry for changing the number of bits of read and write data, for simultaneously inputting and outputting read and write data, for simultaneously transferring read and write data, and that the first unidirectional bus transfers the write data, control signal and address signal through a common data bus line. None of the features are disclosed or suggested by Chappel. Namely, Chappell explains that the bit width and delay are different for each "address bus" that selects the sub-array, the word line, and the bit lines. However, there is no disclosure or suggestion of circuitry related to the read and write data, and respective bit widths, and configurations of common data busses, as claims 10-14 recite.

For the above reasons, Applicant submits that Chappell fails to disclose or suggest each and every element of any one of claims 4 and 10-14 (Applicant acknowledges that the Examiner indicated so for claim 10).

Conclusion

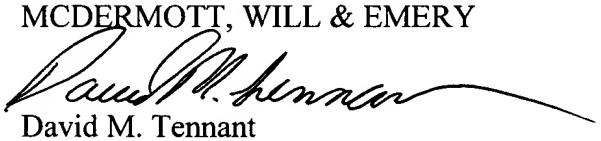
For these reasons, the application should be considered in condition for allowance and passed to issue. Withdrawal of the rejection is respectfully solicited.

If there are any questions regarding this response or the application in general, a telephone call to the undersigned attorney would be appreciated to expedite prosecution of this case. We look forward to receiving your next correspondence.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX SHOWING CHANGES MADE

IN THE CLAIMS

Claims 3, 4 and 15 were amended as follows:

3. (Amended) [The] A semiconductor memory device [according to claim 1,] comprising:

a plurality of input terminals for receiving write data, a control signal and an address signal; and

at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data, wherein the input terminals are coupled to a first bus, and said at least one output terminal is coupled to a second bus, and each of the first and second buses is a unidirectional bus for transferring a signal or data in one direction.

4. (Amended) [The] A semiconductor memory device [according to claim 1, further] comprising:

a plurality of input terminals for receiving write data, a control signal and an address signal;

at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data,

a write conversion circuit coupled between an internal data bus and the input terminal(s) for converting write data applied to said input terminal(s) into internal write data being equal in bit width to said internal data bus, and outputting said internal write data; and

a read conversion circuit coupled between said internal data bus and the output terminal for converting internal read data read onto said internal data bus into data being equal in bit width to said at least one output terminal, and transferring converted data to said at least one output terminal.

15. (Amended) The semiconductor memory device according to claim [1] 3, wherein the input terminals receive the write data, the control signal and the address signal at common terminals.